

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent No.: 6,888,190 62 Issue Date: 05/03/2005
5 App. No.: 10/707,080 Filing Date: 11/20/2003
Inventors: Ching-Sung Yang et al.
Examiner: Jerome Jackson Art Unit: 2815
Docket No.: EMEP0029USA4

10 Title: EEPROM WITH SOURCE LINE VOLTAGE STABILIZATION
MECHANISM

To: Commissioner for Patents
P.O. BOX 1450
Alexandria, VA 22313-1450

15 Subject: Request for Certificate of Correction under 37 CFR 1.322

Dear Sir,

20 Upon reviewing the above-identified patent, patentee noted the status of the
parent application of above-identified patent should be corrected. The parent
application has been patented on 01/25/2005 (see Attachment, the front page of the
Patent No. 6,847,087) and it indicates this as an Office mistake of consequence. As
the agent of record, I hereby request that a Certificate of Correction be issued under
25 37 CFR 1.322 to correct the status of the parent application from "abandoned" to
"patented".

JUL 18 2005

Respectfully submitted,

Winston Hsu

Date: JUL 15 2005

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US006888190B2

(12) **United States Patent**
Yang et al.

(10) **Patent No.:** US 6,888,190 B2
(45) **Date of Patent:** May 3, 2005

(54) **EEPROM WITH SOURCE LINE VOLTAGE STABILIZATION MECHANISM**

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(*) **Notice:** Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) **Appl. No.:** 10/707,080

(22) **Filed:** Nov. 20, 2003

(65) **Prior Publication Data**

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Related U.S. Application Data

(63) Continuation-in-part of application No. 10/065,591, filed on Oct. 31, 2002, now abandoned.

(51) **Int. Cl.**⁷ H01L 29/76; H01L 29/78; H01L 29/788

(52) **U.S. Cl.** 257/314; 257/314; 257/315; 257/316; 257/319; 257/320

(58) **Field of Search** 257/314-320

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Primary Examiner—Jerome Jackson

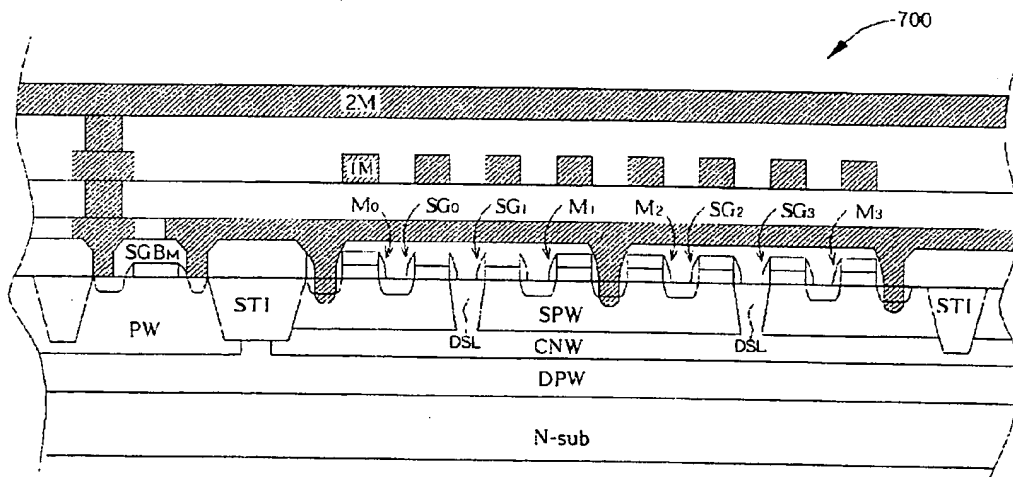
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(57) **ABSTRACT**

A low-voltage nonvolatile memory array includes an N type semiconductor substrate having a memory region. A deep P well is formed in the semiconductor substrate. A cell N well is located within the memory region in the semiconductor substrate. The cell N well is situated above the deep ion well. A shallow P well serving as a buried bit line is doped within the cell ion well. The shallow P well is isolated by an STI layer, wherein the STI layer has a thickness greater than a well depth of the shallow ion well. At least one memory transistor with a stacked gate, a source, and a drain is formed on the shallow ion well. The source of the memory transistor is electrically coupled to the cell N well to induce a capacitor between the cell N well and the deep P well during a read operation, thereby avoiding read current bounce or potential power crash. A bit line overlies the memory transistor and is electrically connected to the drain of the memory transistor via a bit line contact plug short-circuiting the drain of the memory transistor and the shallow P well.

15 Claims, 29 Drawing Sheets



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patent application 10/10/08

EME-39



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(12) United States Patent
Yang et al.**(10) Patent No.: US 6,847,087 B2****(45) Date of Patent: *Jan. 25, 2005****(54) BI-DIRECTIONAL FOWLER-NORDHEIM
TUNNELING FLASH MEMORY****(75) Inventors:** Ching-Sung Yang, Chang-Hua Hsien
(TW); Shih-Jye Shen, Hsin-Chu (TW);
Ching-Hsiang Hsu, Hsin-Chu (TW)**(73) Assignee:** eMemory Technology Inc., Hsin Chu
(TW)**(*) Notice:** Subject to any disclaimer, the term of this
patent is extended or adjusted under 35
U.S.C. 154(b) by 175 days.This patent is subject to a terminal dis-
claimer.**(21) Appl. No.: 10/065,591****(22) Filed: Oct. 31, 2002****(65) Prior Publication Data**

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(51) Int. Cl.⁷ H01L 29/76; H01L 29/94;
H01L 31/062; H01L 31/113; H01L 31/119**(52) U.S. Cl.** 257/390; 257/315; 257/316;
257/318; 257/390**(58) Field of Search** 257/208, 314-316,
257/318, 319, 322, 390, 391**(56) References Cited****U.S. PATENT DOCUMENTS**

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Primary Examiner—Tom Thomas**Assistant Examiner**—Jesse A. Fenty**(74) Attorney, Agent, or Firm**—Winston Hsu**(57) ABSTRACT**

A low-voltage nonvolatile memory array includes a cell well of a first conductivity type formed in a substrate; columns of buried bit lines of a second conductivity type formed within the cell well, wherein columns of the buried bit lines are isolated from each other and each is further divided into of sub-bit line segments with deeply doped source wells of the first conductivity type connected to the cell well; a plurality of memory cell blocks serially arranged over one of the columns of buried bit lines, wherein a memory cell block corresponds to a sub-bit line segment, and each memory cell block includes at least one memory transistor having a stacked gate, source, and drain; and a local bit line overlying the memory cell blocks and electrically connected to the drain of the memory transistor via a contact plug short-circuiting the drain and the subjacent buried bit line.

21 Claims, 24 Drawing Sheets